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S1D13513 Display Controller

S5U13513P00C100 Evaluation Board User Manual

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Table of Contents

1 Introduction

This manual describes the setup and operation of the S5U13513P00C100 Evaluation Board. The evaluation board is designed as an evaluation platform for the S1D13513 Display Controller.

The S5U13513P00C100 evaluation board can connect to the S5U13U00P00C100 USB Adapter board so that it can be used with a laptop or desktop computer, via USB 2.0. With some minor modifications, it is possible to connect the S5U13513P00C100 evaluation board to a Epson PC Card Extender board instead of a USB Adapter board. The S5U13513P00C100 evaluation board can also be used with many other native platforms via the host connectors which provide the appropriate signals to support a variety of CPUs.

This user manual is updated as appropriate. Please check the Epson Research and Development Website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Features

The S5U13513P00C100 Evaluation Board includes the following features:

- 256-pin PBGA S1D13513 Display Controller
- On-board SDRAM, selectable as 8MB x 32-bit or 8MB x 16-bit
- Headers for connection to the S5U13U00P00C100 USB Adapter board or to the PC Card Extender board
- Headers for connecting to various Host Bus Interfaces
- Headers for connecting to LCD panels
- Headers for connecting to cameras
- On-board 10MHz crystal (used for OSC1 clock input)
- On-board 27MHz crystal (used for OSC2 clock input)
- 14-pin DIP socket (used to install an oscillator for CLKI3 clock input)
- 3.3V input power
- On-board voltage regulator with 1.8V output

3 Installation and Configuration

The S5U13513P00C100 evaluation board incorporates a DIP switch, jumpers, and 0 ohm resistors which allow it to be used with a variety of different configurations.

3.1 Configuration DIP Switch

The S1D13513 has configuration inputs (CNF[8:0]) which are read on the rising edge of RESET#. A 10-position DIP switch (SW1) is used to configure the S1D13513 for multiple Host Bus Interfaces. The following figure shows the location of DIP switch SW1 on the S5U13513P00C100.

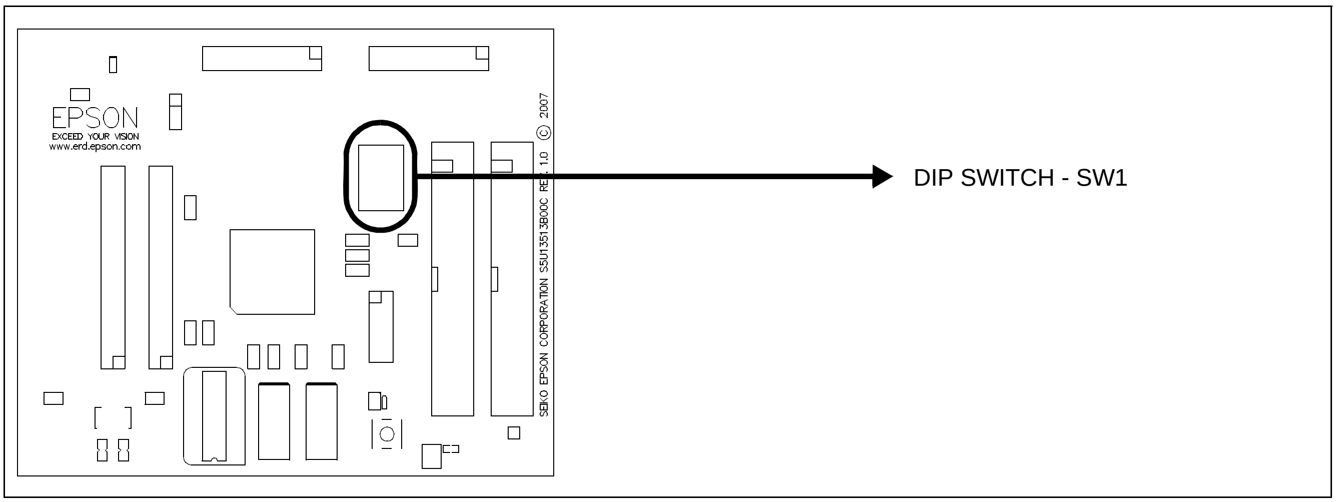


Figure 3-1: Configuration DIP Switch (SW1) Location

All S1D13513 configuration inputs (CNF[8:0]) are fully configurable using DIP switch SW1 as described below.

Table 3-1: Summary of Power-On/Reset Options

SDU13513B00C SW1-[10:1] Config	S1D13513 CNF[8:0] Config	Power-On/Reset State	
		1 (ON)	**0 (OFF)**
SW1-[10]	-	Not used	
SW1-[9:8]	CNF[8:7]	00b	CLKI3 is the PLL1 clock source
		01b	BUSCLK is the PLL1 clock source
		10b	OSC1 is the PLL1 clock source
		11b	OSC2 is the PLL1 clock source
SW1-[6]	CNF5	Indirect access	Direct access
SW1-[7]	CNF6	See Table 3-2: “CNF[4:0] Setting for CNF[6] = 1b”	See Table 3-3: “CNF[4:0] Setting for CNF[6] = 0b”
SW1-[5:1]	CNF[4:0]	00000b	Parallel Direct 80 Type 2: 1CS# (see Table 3-2: “CNF[4:0] Setting for CNF[6] = 1b”)

(highlighted) = Required settings when using S5U13U00P00C100 USB Adapter board (SW1-[9:1] = 101000000b)

Table 3-2: CNF[4:0] Setting for CNF[6] = 1b

CNF[4:0]	Host Bus
00000b	Parallel Direct 80 Type 2: 1 CS#
00001b	Parallel Direct 80 Type 3: 1 CS#
00010b	Parallel Indirect 80 Type 2
00011b	Parallel Indirect 80 Type 3
00100b	Parallel Direct 80 Type 1: 1 CS#
00101b	Parallel Direct 68: 1 CS#
00110b	Parallel Indirect 80 Type 1
00111b	Parallel Indirect 68
01000b	Parallel Direct 80 Type 2: 2 CS#
01001b	Parallel Direct 80 Type 3: 2 CS#
01010b	Reserved
01011b	Reserved
01100b	Parallel Direct 80 Type 1: 2 CS#
01101b	Parallel Direct 68: 2 CS#
01110b	Reserved
01111b	Reserved
10000b	Serial on HVDD1: Data valid on falling edge
10001b	Serial on HVDD2: Data valid on falling edge
10010b	Reserved
10011b	Reserved
10100b	Reserved
10101b	Reserved
10110b	Reserved
10111b	Reserved
11000b	Serial on HVDD1: Data valid on rising edge
11001b	Serial on HVDD2: Data valid on rising edge
11010b	Reserved
11011b	Reserved
11100b	Reserved
11101b	Reserved
11110b	Reserved
11111b	Reserved

	= Required settings when using S5U13U00P00C100 USB Adapter board (SW1-[9:1] = 101000000b)

Table 3-3: CNF[4:0] Setting for CNF[6] = 0b

CNF[4:0]	Host Bus
00000b	Generic Little Endian: Active Low WAIT# with tri-state
00001b	Generic Little Endian: Active Low WAIT# always driven
00010b	Generic Little Endian: Active HIgh WAIT# with tri-state
00011b	Reserved
00100b	Generic Big Endian: Active Low WAIT# with tri-state
00101b	Generic Big Endian: Active Low WAIT# always driven
00110b	Generic Big Endian: Active HIgh WAIT# with tri-state
00111b	Reserved
01000b	MIPS/ISA Little Endian: Active Low WAIT# with tri-state
01001b	MIPS/ISA Little Endian: Active Low WAIT# always driven
01010b	MIPS/ISA Little Endian: Active HIgh WAIT# with tri-state
01011b	Reserved
01100b	MC68000 Big Endian: Active High WAIT# with tri-state
01101b	Reserved
01110b	MC68030 Big Endian: Active High WAIT# with tri-state
01111b	Reserved
10000b	PR31500/31700/TX3912 Little Endian: Active Low WAIT# with tri-state (16-bit memory accesses only)
10001b	PR31500/31700/TX3912 Little Endian: Active Low WAIT# always driven (16-bit memory accesses only)
10010b	Reserved
10011b	Reserved
10100b	Reserved
10101b	Reserved
10110b	MPC821/555/556 Big Endian: Active High WAIT# with tri-state
10111b	Reserved
11000b	SH3 Little Endian: Active Low WAIT# with tri-state
11001b	SH3 Little Endian: Active Low WAIT# always driven
11010b	SH4 Little Endian: Active High WAIT# with tri-state
11011b	Reserved
11100b	SH3 Big Endian: Active Low WAIT# with tri-state
11101b	SH3 Big Endian: Active Low WAIT# always driven
11110b	SH4 Big Endian: Active High WAIT# with tri-state
11111b	Reserved

3.2 Configuration Jumpers

The S5U13513P00C100 has 11 jumper blocks which configure various board settings. The jumper positions for each function are shown below.

Table 3-4: Configuration Jumper Summary

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	COREVDD	Normal	—	COREVDD current measurement
JP2	PLLVDD1	Normal	—	PLLVDD1 current measurement
JP3	PLLVDD2	Normal	—	PLLVDD2 current measurement
JP4	OSCVDD1	Normal	—	OSCVDD1 current measurement
JP5	OSCVDD2	Normal	—	OSCVDD2 current measurement
JP6	HVDD1	Normal	—	HVDD1 current measurement
JP7	HVDD2	Normal	—	HVDD2 current measurement
JP8	HVDD3	Normal	—	HVDD3 current measurement
JP9	HVDD4	Normal	—	HVDD4 current measurement
JP10	HVDD5	Normal	—	HVDD5 current measurement
JP11	SDRAM Width Select	32-bit wide SDRAM	16-bit wide SDRAM	—

JP1-JP10 - Power Supplies for the S1D13513

JP1-JP10 can be used to measure current consumption of each S1D13513 power supply. When the jumper is at position 1-2, normal operation is selected.
When no jumper is installed, the current consumption for each power supply can be measured by connecting an ammeter to pin 1 and 2 of the jumper.

The jumper associated to each power supply is as follows:

JP1 for COREVDD
JP2 for PLLVDD1
JP3 for PLLVDD2
JP4 for OSCVDD1
JP5 for OSCVDD2
JP6 for HVDD1 (Host interface)
JP7 for HVDD2 (LCD Panel interface)
JP8 for HVDD3 (Camera2 interface)
JP9 for HVDD4 (Camera1 interface)
JP10 for HVDD5 (SDRAM interface)

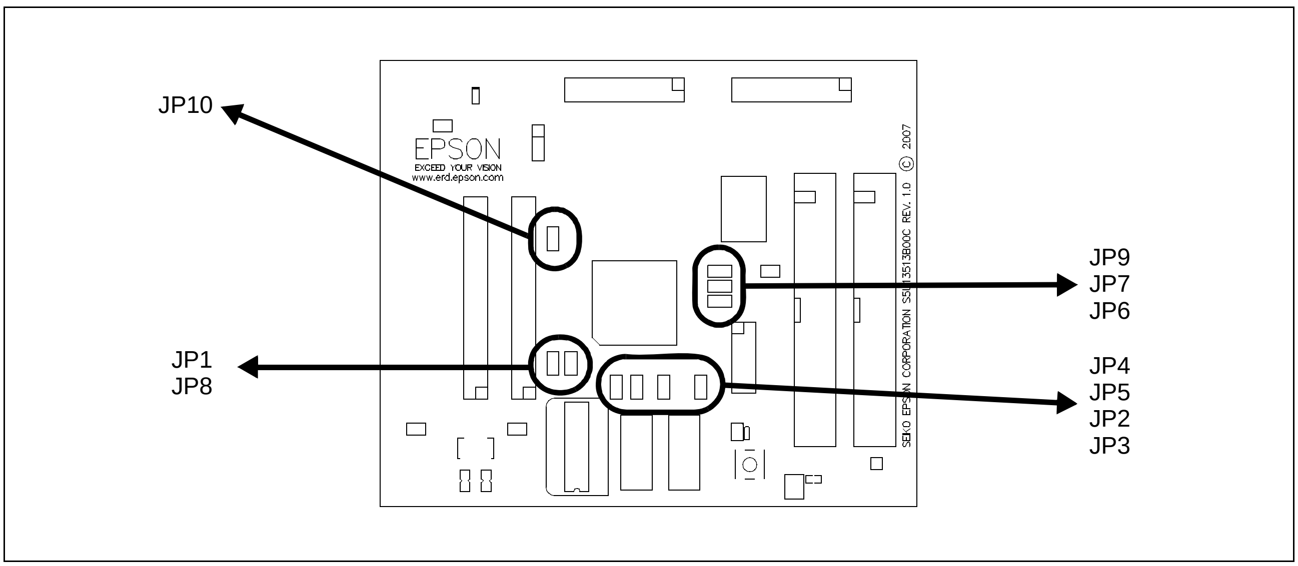


Figure 3-2: Configuration Jumper Locations (JP1-JP10)

JP11 - SDRAM Width Select

JP11 is used to select the bus width of the external SDRAM.
When the jumper is at position 1-2, the external SDRAM is 32-bit wide and memory size is 32MB. The memory consists of 2 chips in parallel, each 16MB and 16-bit wide.
When the jumper is at position 2-3, the external SDRAM is 16-bit wide and memory size is 16MB. In this position one memory chip is disabled and only one chip is active (16MB and 16-bit wide).

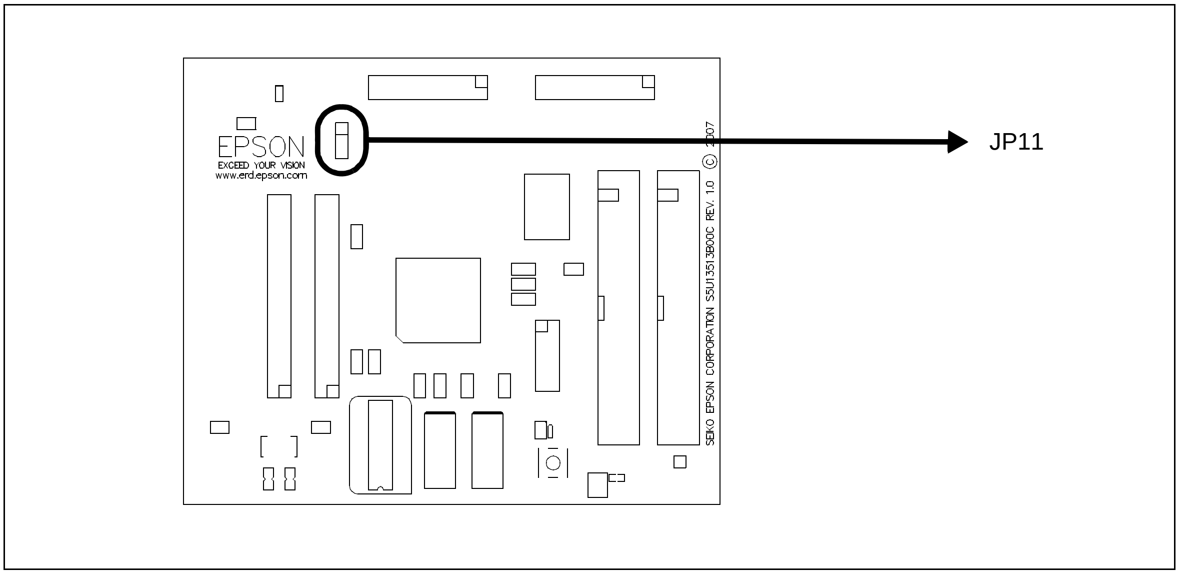


Figure 3-3: Configuration Jumper Location (JP11)

4 Technical Description

4.1 Power

4.1.1 Power Requirements

The S5U13513P00C100 evaluation board requires an external regulated power supply (3.3V at 1A). The power is supplied to the evaluation board through pin 5 of the P2 header, or pin 29 of the H2 header.

The green LED ‘3.3V Power’ is turned on when 3.3V power is applied to the board.

4.1.2 Voltage Regulators

The S5U13513P00C100 evaluation board has an on-board linear regulator to provide the 1.8V power required by the S1D13513 Display Controller.

Additionally, there is a step-up switching voltage regulator to generate 6~24V. This output is adjustable and can be used to power the LED backlight on some LCD panels.

4.1.3 S1D13513 Power

The S1D13513 Display Controller requires 1.8V and 3.3V power supplies.

1.8V power is provided by the on-board linear voltage regulator. It is used for CoreVDD, PLLVDD1, PLLVDD2, OSCVDD1, OSCVDD2.

3.3V power must be provided by the external power supply. It is used for HVDD1 (host interface - HIOVDD), HVDD2 (LCD panel interface - PIOVDD), HVDD3 (camera 2 interface - CIOVDD2), HVDD4 (camera 1 interface - CIOVDD1), and HVDD5 (SDRAM interface).

HIOVDD is connected to 3.3V through a 0 ohm resistor, R31. If it is desired to have a different voltage for HIOVDD, R31 must be removed and the desired supply connected to pin 11 of connector P1.

PIOVDD is connected to 3.3V through a 0 ohm resistor, R33. If it is desired to have a different voltage for PIOVDD, R33 must be removed and the desired supply connected to pin 32 of connector H4.

CIOVDD2 is connected to 3.3V through a 0 ohm resistor, R34. If it is desired to have a different voltage for CIOVDD2, R34 must be removed and the desired supply connected to pin 15 of connector H7.

CIOVDD1 is connected to 3.3V through a 0 ohm resistor, R70. If it is desired to have a different voltage for CIOVDD1, R70 must be removed and the desired supply connected to pin 15 of connector H6.

HVDD5 is always connected to 3.3V.

Note

The recommended range for HVDD1 (HIOVDD), HVDD2 (PIOVDD), HVDD3 CIOVDD2), and HVDD4 (CIOVDD1) is 3.0V~3.6V.

4.2 Clocks

S1D13513 has four clock inputs: BUSCLK, OSC1, OSC2 and CLKI3. BUSCLK and CLKI3 require a clock provided by an external oscillator. OSC1 and OSC2 have an internal oscillator and can work with a crystal or with an external oscillator.

For the S5U13513P00C100 evaluation board, OSC1 and OSC2 use crystals (10MHz for OSC1 and 27MHz for OSC2).

For the S5U13513P00C100 evaluation board, CLKI3 is not used and is pulled to ground by a 10kΩ resistor. However, if CLKI3 is required, connect a 14-pin, DIP package oscillator in the Y1 footprint.

For the S5U13513P00C100 evaluation board, BUSCLK is not used and is pulled to ground by a 10kΩ resistor. However, if BUSCLK is required, the BUSCLK pin is connected to the H2 connector and to the P1 connector where it may be provided by the host development platform.

4.3 Reset

The S5U13513P00C100 evaluation board can be reset using a push-button, or via an active low reset signal from the host development platform (see H2 connector or P1 connector).

The reset signal will reset the S1D13513 Display Controller and is available on the H6 and H7 connectors. It is possible to remove the reset signal from the H6 and H7 connectors by removing the 0 Ohm resistor R80 from the board.

4.4 Host Interface

4.4.1 Connecting to the Epson S5U13U00P00C100 USB Adapter Board

The S5U13513P00C100 evaluation board is designed to connect to a S5U13U00P00C100 USB Adapter Board. The USB adapter board provides a simple connection to any computer via a USB 2.0 connection. The S5U13513P00C100 directly connects to the adapter board through connectors P1 and P2. The USB adapter board also supplies the 3.3V power required by the S5U13513P00C100.

4.4.2 Connecting to the Epson PC Card Extender Board

The S5U13513P00C100 evaluation board may be connected to an Epson PC Card Extender Board, but it will require an external 3.3V power supply and some modifications to the S5U13513P00C100 board.

The modifications required for the S5U13513P00C100 board are:

1. Remove R107 and R108 (0 ohm resistors, size 0603)
2. Remove R109 and R112 (0 ohm resistors, size 0402)
3. Populate R110 and R111 with 0 ohm resistors, size 0402 (or short the pads on the board)
4. Set DIP switch SW1-[5:1] to 00100b (CNF[4:0]=00100b) to select Parallel Direct 80 Type 1: 1CS# host interface

To use a modified S5U13513P00C100 with an Epson PC Card Extender board:

1. Connect the 2 boards using connectors P1 and P2.
2. Connect 3.3V power supply to the S5U13513P00C100. Connect the positive of the power supply to test point TP3.3VDD1, and the negative to test point TPGND2
3. Plug the PC Card Extender (with S5U13513P00C100 connected to it) into a PC Card slot on a PC.
4. Turn on the 3.3V power supply and the S5U13513P00C100 is ready to use. Note that a windows driver is required to be installed on the PC (the S1D13xxx PCI/PC Card Bus driver is available from www.erd.epson.com).

4.4.3 Direct Host Bus Interface Support

The S1D13513 Display Controller directly supports many host bus interfaces. For detailed S1D13513 pin mapping, refer to the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

All S1D13513 host interface pins are available on connectors H2 and H3 which allow the S5U13513P00C100 to be connected to a variety of development platforms. However, connectors H2 and H3 are not populated on the S5U13513P00C100 evaluation board.

If connectors H2 and H3 are added, all host interface signals must match HVDD1 of the S1D13513. For the maximum/minimum values of the voltages, refer to the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

The following diagram shows the location of the host bus connectors, H2 and H3. They are 0.1x0.1” 34-pin headers (17x2).

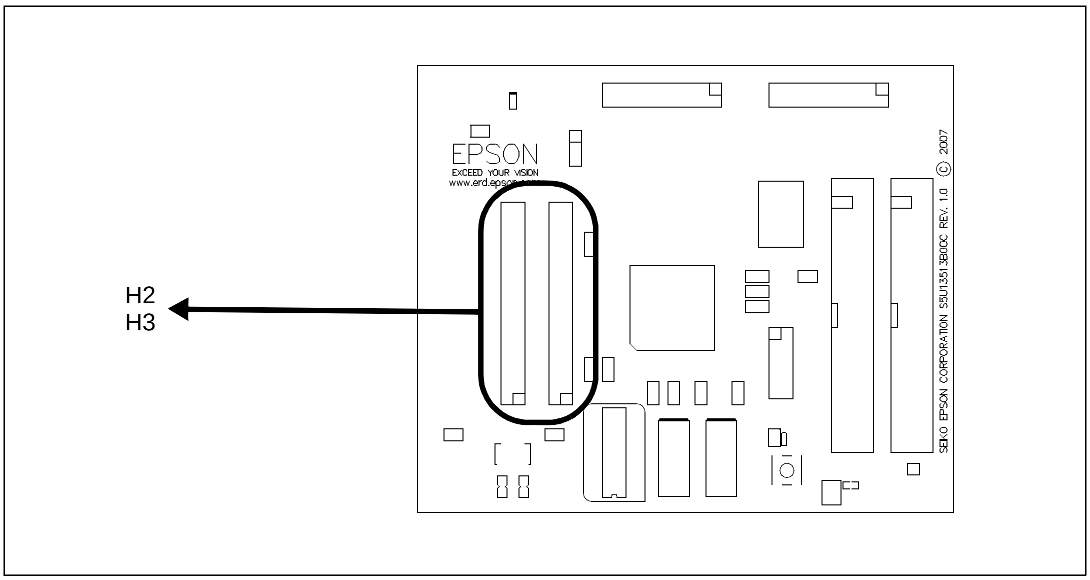


Figure 4-1: Host Bus Connector Locations (H2 and H3)

For the pinout of connectors H2 and H3, see “Schematic Diagrams” on page 24.

4.5 LCD Panel Interface

The LCD interface signals are available on connectors H4 and H5. Connector H5 includes GPIOG[4:0] which may be used as additional signals for extended TFT interfaces. For S1D13513 LCD interface pin mapping, refer to the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Connectors H4 and H5 are both 0.1x0.1" 40-pin headers (20x2). For the pinout of connectors H4 and H5, see "Schematic Diagrams" on page 24.

On the evaluation board there is an adjustable 6~24V, 40mA max. power supply. This voltage is provided only on connector H4 (it is not used elsewhere on the board). It is intended for use to power the LED backlight on some LCD panels. The voltage is adjusted by the R106 pot.

Note

For LCD panels that use CCFL backlight, an external power supply must be used to provide power to the inverter for CCFL backlight. Usually, the inverter current consumption is higher than the maximum 40mA current available from the on-board voltage regulator.

The following diagram shows the location of the LCD panel connectors H4 and H5.

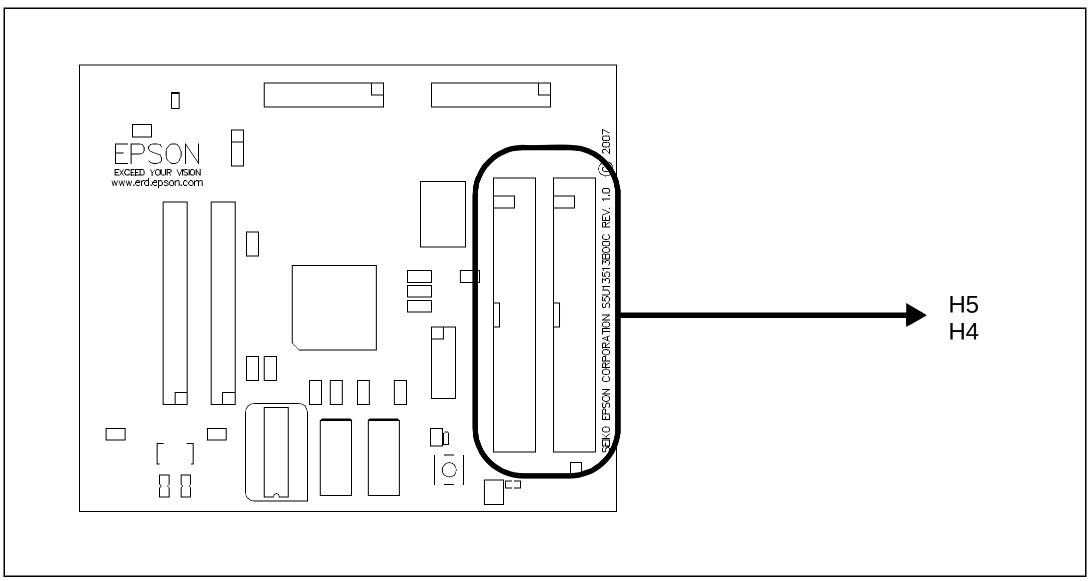


Figure 4-2: LCD Panel Connectors Locations (H4, H5)

4.6 Camera Interface

All the signals for the Camera1 interface are available on connector H6. All the signals for the Camera2 interface are available on connector H7. H6 and H7 are 0.1x0.1” 20-pin headers (10x2). For the pinout of connectors H6 and H7, see “Schematic Diagrams” on page 24.

The S1D13513 Camera1 interface signals use the GPIOC[7:0] and GPIOD[3:0] pins. The Camera2 interface signals use the GPIOA[7:0] and GPIOB[7:0] pins. These GPIO pins may be configured for a variety of S1D13513 supported functions. GPIOC[7:0] and GPIOD[3:0] may be configured as GPIO pins, Camera1 interface pins, or as YUV output pins. GPIOA[7:0] and GPIOB[7:0] may be configured as GPIO pins, Camera2 interface pins, Keypad interface pins, or PWM output pins. For detailed S1D13513 GPIO pin mapping, refer to the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Connector H6 and H7 may be used to evaluate any function for which the GPIOA[7:0], GPIOB[7:0], GPIOC[7:0], GPIOD[3:0] can be configured.

The S1D13513 has an I2C interface which uses two signals that are connected to both the H6 and H7 connectors. The default configuration of the evaluation board has the I2C signals, I2C_SCL and I2C_SDA, pulled high to CIOVDD1. If the I2C signals must be pulled high to CIOVDD2, R162 and R175 must be removed and 4.7kΩ resistors must be mounted for R164 and R177.

The reset signal provided on H6 and H7 is active low and is pulled to HIOVDD when inactive.

The following diagram shows the location of the camera connectors H6 and H7.

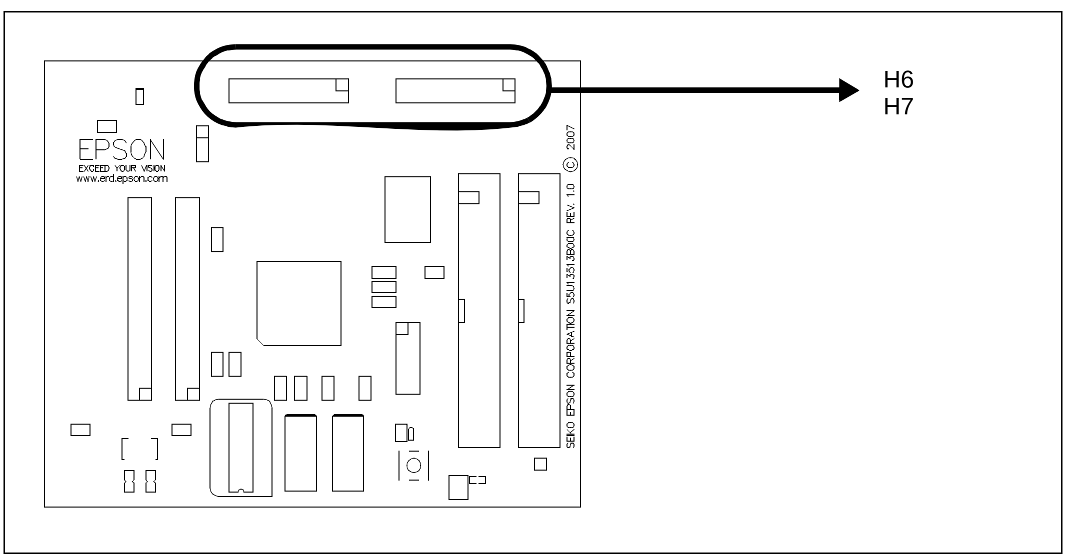


Figure 4-3: Camera Expansion Connector Locations (H6, H7)

4.7 YUV Output for TV Display

The S1D13513 can output YUV data which can be used to display an image on a TV screen via an external video encoder. The YUV output is multiplexed with other functions on the GPIOC[7:0] and GPIOD[2:0] pins. These pins are routed to connector H6.

4.8 Keypad Interface

The S1D13513 has a 5x5 keypad interface which is multiplexed with other functions on the GPIOA[4:0] and GPIOB[4:0] pins. These pins are routed to connectors H6 and H7. It is possible to use a Keypad device with the S5U13513P00C100 evaluation board by connecting it to the H6 and H7 connectors.

4.9 PWM Outputs

The S1D13513 has 4 PWM outputs which may be used to control the brightness of 4 LEDs. It also has an input, AUDIN, which is used to control the overall operation of the PWM outputs. The PWM output function is multiplexed on the GPIOA[7:5] and GPIOB[7] pins. AUDIN is multiplexed on the GPIOD[3] pin. These pins are routed to connector H6 and H7.

4.10 GPIO Connections

The S1D13513 Display Controller GPIO pins have multiple functions. All the GPIO pins are routed to the connectors on the S5U13513P00C100 evaluation board. If any pin is configured as a GPIO, it will be available on the connectors as listed below:

GPIOA[7:0] pins are routed to connector H7.

GPIOB[7:5] and GPIOB[3:0] pins are routed to connector H7. GPIOB[6:5] are also routed to connector H6.

GPIOB[4] pin is routed to connector H6.

GPIOC[7:0] pins are routed to connector H6.

GPIOD[3:0] pins are routed to connector H6.

GPIOG[4:0] pins are routed to connector H5.

FPDAT[23:18] which may be used as GPIOH[5:0] are routed to connector H5.

4.11 JTAG Connector

The S1D13513 design includes a JTAG interface. All the JTAG signals are available on connector H1, however, connector H1 is not populated on the board. For the pinout of connector H1, see “Schematic Diagrams” on page 24.

The following diagram shows the location of the JTAG connector (H1).

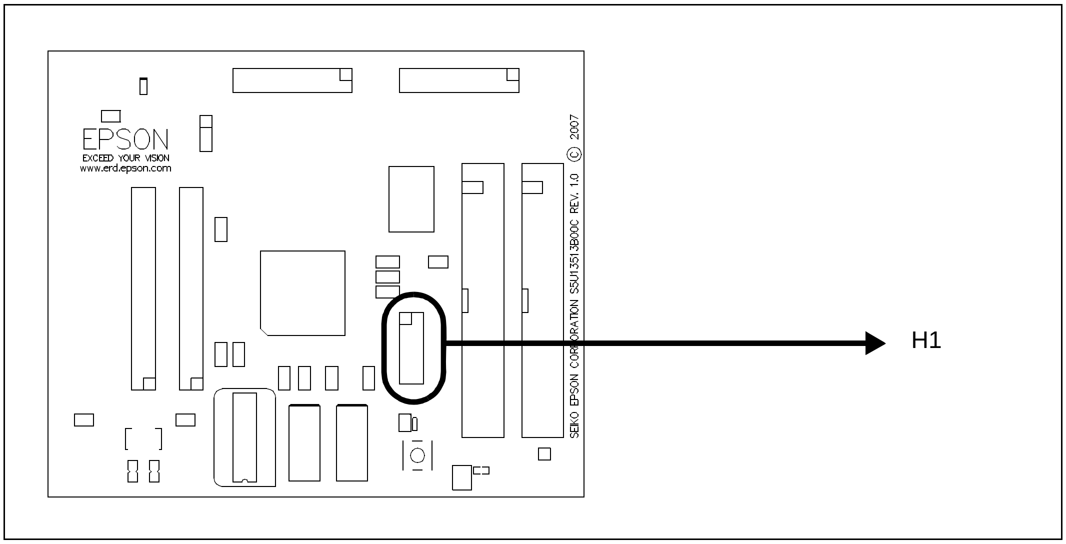


Figure 4-4: JTAG Connector Location

5 Parts List

Table 5-1: Parts List

Item	Qty	Reference	Part	Description	Manufacturer / Part No. / Assembly Instructions
1	49	C1, C2, C3, C4, C5, C6, C7, C8, C9, C19, C22, C26, C28, C29, C30, C31, C32, C33, C34, C35, C43, C44, C45, C46, C47, C48, C49, C50, C51, C65, C66, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C98, C100, C104, C105	0.1uF		Yageo America 04022F104Z7B20D
2	41	C10, C11, C12, C13, C14, C15, C16, C17, C18, C25, C27, C36, C37, C38, C39, C40, C41, C42, C52, C53, C54, C55, C56, C57, C58, C59, C60, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96	0.01uF		Yageo America 0402ZRY5V7BB103
3	2	C20, C23	1nF		Yageo America 04022R102K9B20D
4	2	C21, C24	10uF		Panasonic - ECG ECJ-CV50J106M
5	4	C61, C62, C63, C64	18pF		Panasonic - ECG ECJ-0EC1H180J
6	2	C67, C68	10uF		Panasonic - ECG ECJ-2FB1A106K
7	2	C97, C99	1uF		Panasonic - ECG ECJ-0EB0J105M
8	1	C101	4.7uF 10V T		Kemet T491B475K010AS
9	1	C102	10pF		Panasonic - ECG ECJ-0EC1H100D
10	1	C103	1uF 50V		TDK C3216X7R1H105K
11	1	D1	DIODE	DIODE SCHOTTKY 20V100MA SSSMINI2	Panasonic - SSG MA27D2700L
12	1	D2	3.3V Power	LED GREEN SS TYPE LOW CUR SMD	Panasonic - SSG LNJ308G8LRA
13	1	D3	MBR0530		Micro Commercial Co. MBR0530-TP
14	2	F1, F2	ACF451832-222	FILTER 3-TERM 60MHZ 300MA SMD	TDK ACF451832-222
15	0	H1	HEADER 6X2		Samtec TSW-106-05-G-D
16	0	H2, H3	HEADER_17X2		AMP 1-87215-7
17	1	H4	LCD Connector		Samtec TST-120-01-G-D
18	1	H5	Extended LCD Connector		Samtec TST-120-01-G-D

Table 5-1: Parts List

Item	Qty	Reference	Part	Description	Manufacturer / Part No. / Assembly Instructions
19	2	H6, H7	HEADER_10X2		Samtec TSW-110-05-G-D
20	10	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10		CONN HEADER VERT 2POS .100 TIN or GENERIC	
21	1	JP11	HEADER 3	CONN HEADER VERT 3POS .100 TIN or GENERIC	
22	9	L1, L2, L3, L4, L5, L6, L7, L8, L9	Ferrite	FERRITE 200MA 938 OHMS 0603 SMD	Steward HZ0603B751R-10
23	1	L10	10uH	COIL 10UH 1300MA CHOKE SMD	Panasonic - ECG ELL-6SH100M
24	2	P1, P2	HEADER_20X2		3M 151240-8422-RB
25	58	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R32, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R68, R69, R77	33 1%		
26	7	R31, R33, R34, R70, R96, R107, R108	0		
27	12	R59, R60, R61, R62, R63, R64, R65, R66, R67, R78, R79, R81	10k		
28	6	R71, R76, R80, R102, R109, R112	0		
29	2	R72, R73	1M		
30	2	R74, R75	220		
31	1	R82	270 1%		
32	15	R83, R85, R87, R88, R89, R90, R91, R92, R93, R94, R95, R97, R99, R101, R105	47k		
33	2	R84, R98	4.7k		
34	0	R86, R100, R110, R111	NP		
35	1	R103	887k 1%		
36	1	R104	22k		
37	1	R106	200k		Panasonic - ECG EVN-5ESX50B25
38	11	SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9, SH10, SH11	.100 in. Jumper Shunt	JUMPER SHORTING TIN	Sullins Electronics Corp. STC02SYAN

Table 5-1: Parts List

Item	Qty	Reference	Part	Description	Manufacturer / Part No. / Assembly Instructions
39	1	SW1	SW DIP-10		CTS 218-10LPST
40	1	SW2	SW TACT-SPST	SWITCH TACT SILVER PLT GULLWING	ITT Industries KSC241GLFS
41	4	TPGND1, TPGND2, TPGND3, TP3.3VDD1	TP_SMT	PC TEST POINT MINIATURE SMT	Keystone 5015
42	0	T1	TP SIP		
43	1	U1	S1D13513 PBGA256		
44	2	U2, U3	IS42S16800D-7TL	alternate Micron MT48LC8M16A2P-7E	ISSI IS42S16800D-7TL
45	1	U4	TPS3801L30DCKR	IC 2.64V SUPPLY MON SOT-323-5	Texas Instruments TPS3801L30DCKR
46	1	U5	MIC37100-1.8WS	Alternate MIC39100-1.8WS	Micrel MIC37100-1.8WS
47	1	U6	TPS61040	IC CONV DC/DC BOOST LP SOT-23-5	TI TPS61040DVBR
48	1	X1	MA-506 10.0000M		
49	1	X2	MA-506 27.0000M		
50	0	Y1	14-Pin DIP		AMP 2-641609-1

6 Schematic Diagrams

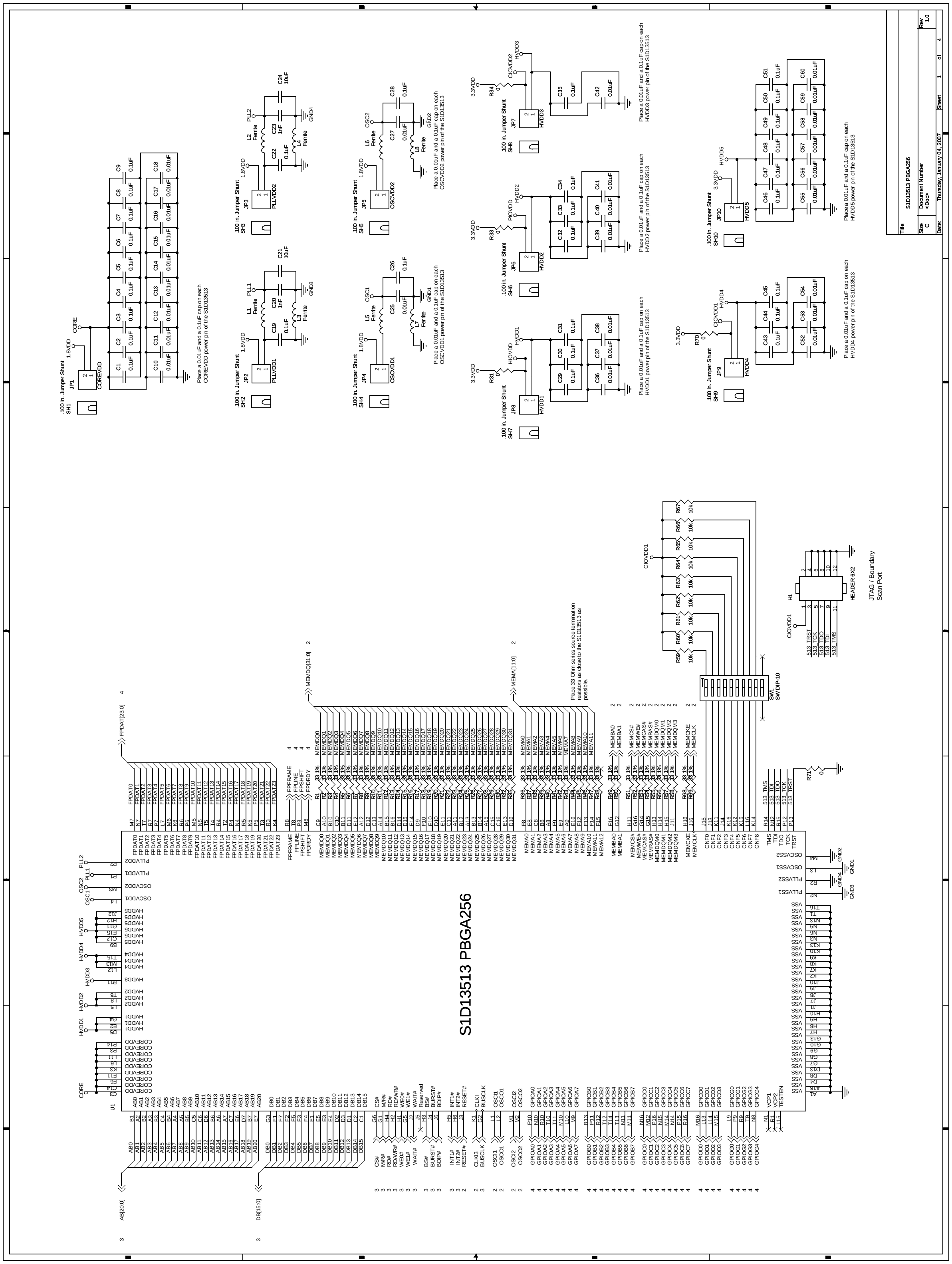


Figure 6-1: S5U13513P00C100 Schematics (1 of 4)

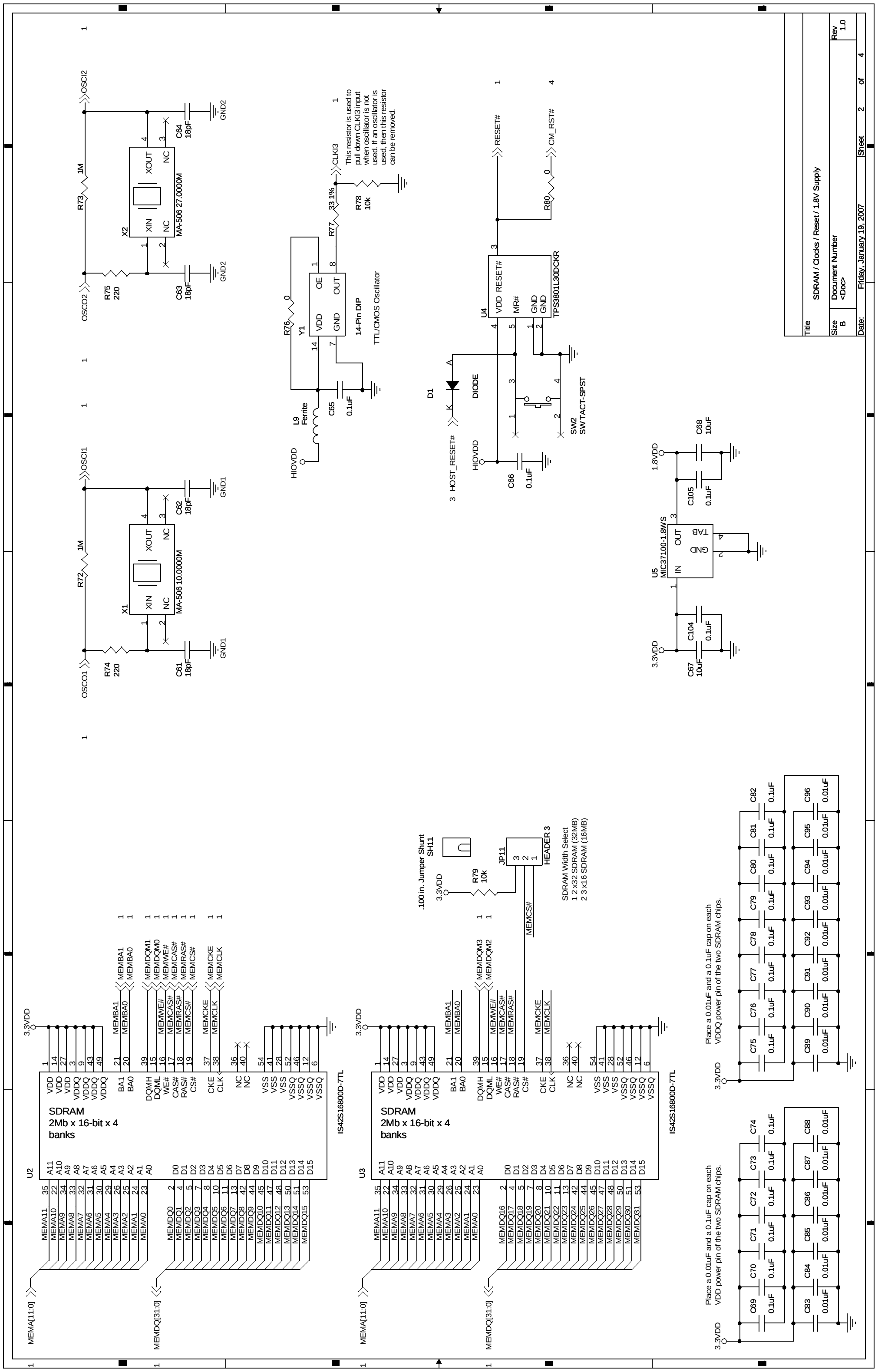


Figure 6-2: S5U13513P00C100 Schematics (2 of 4)

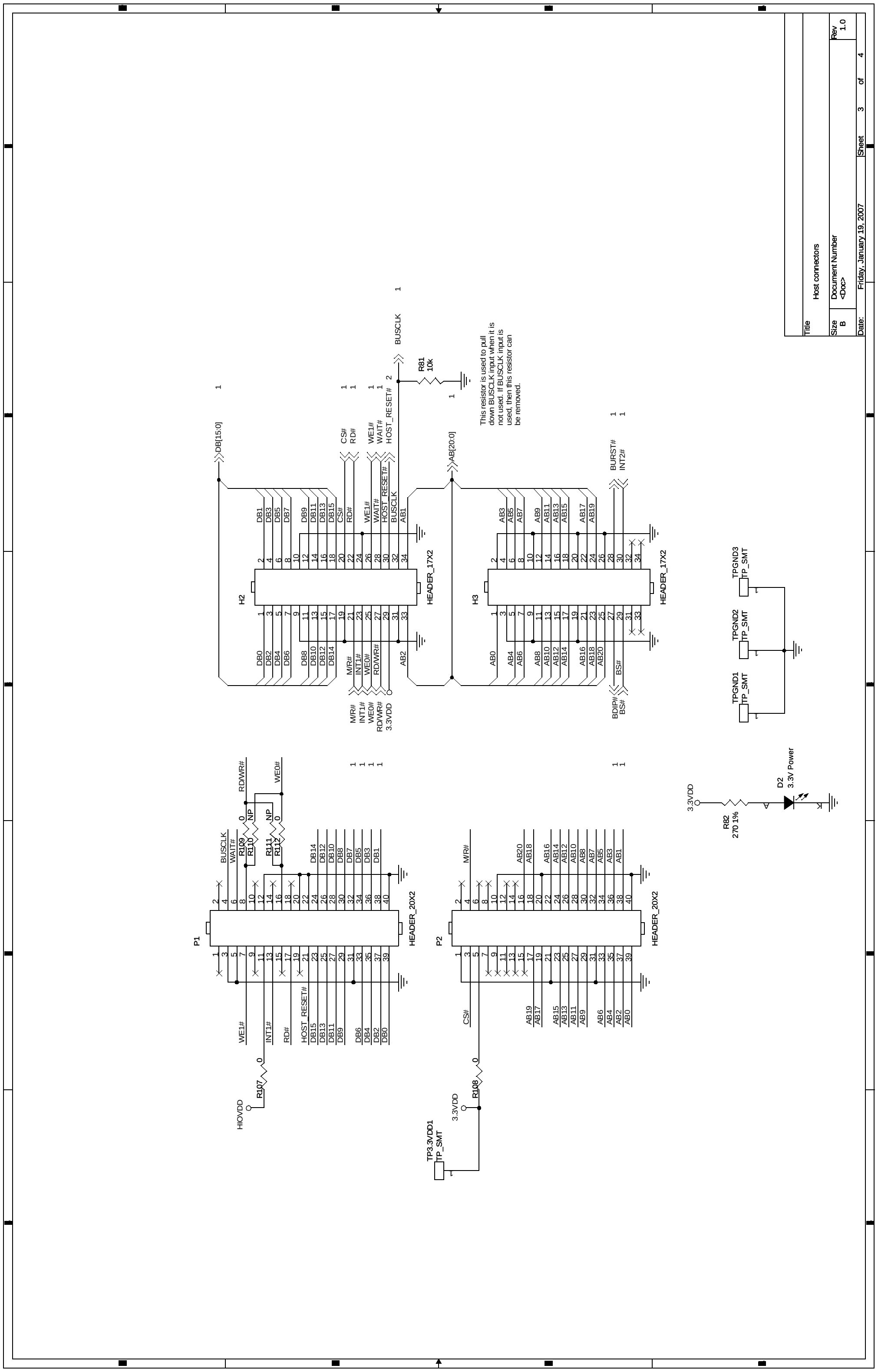


Figure 6-3: S5U13513P00C100 Schematics (3 of 4)

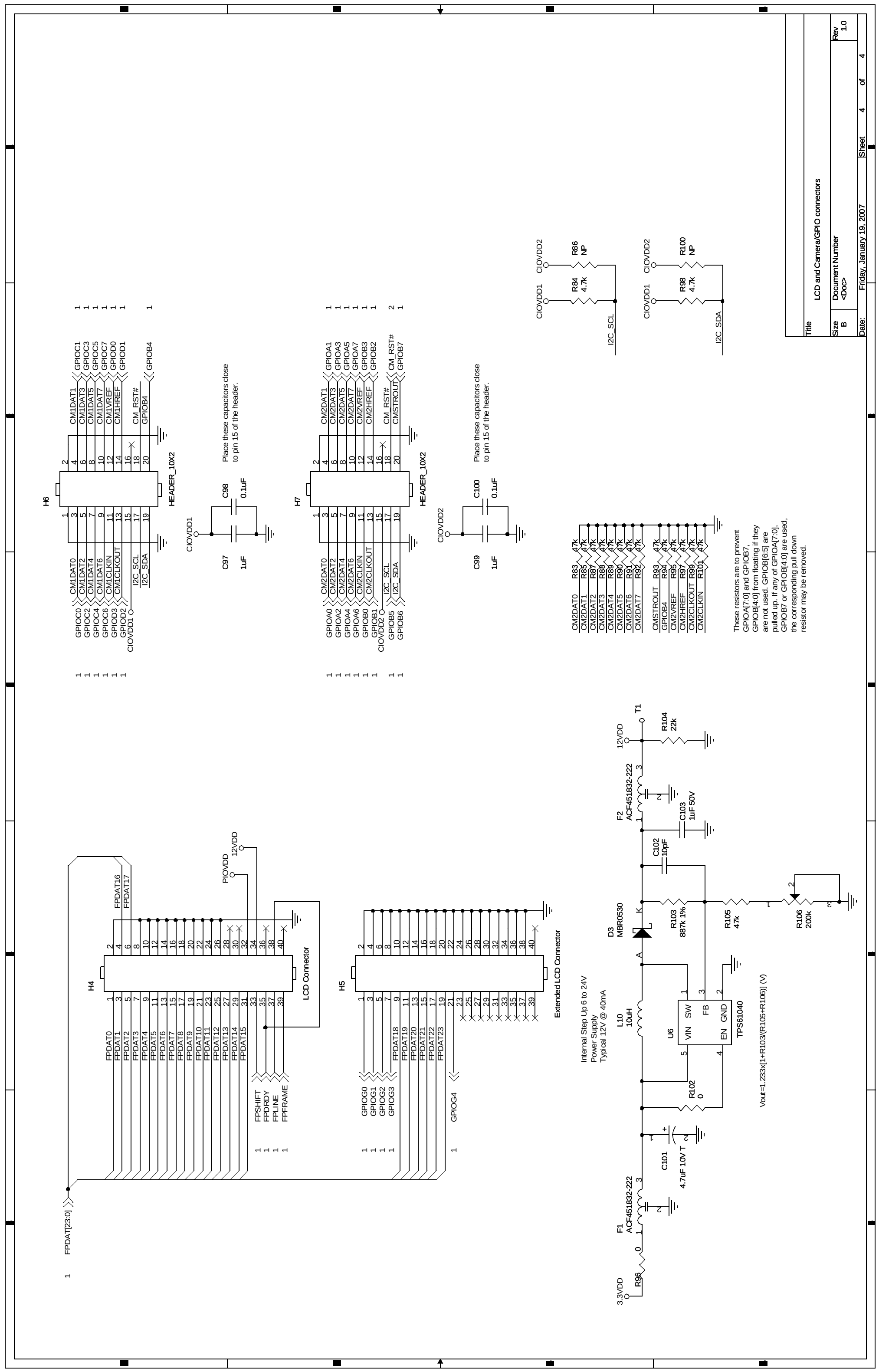


Figure 6-4: S5U13513P00C100 Schematics (4 of 4)

7 S5U13513P00C100 Board Layout

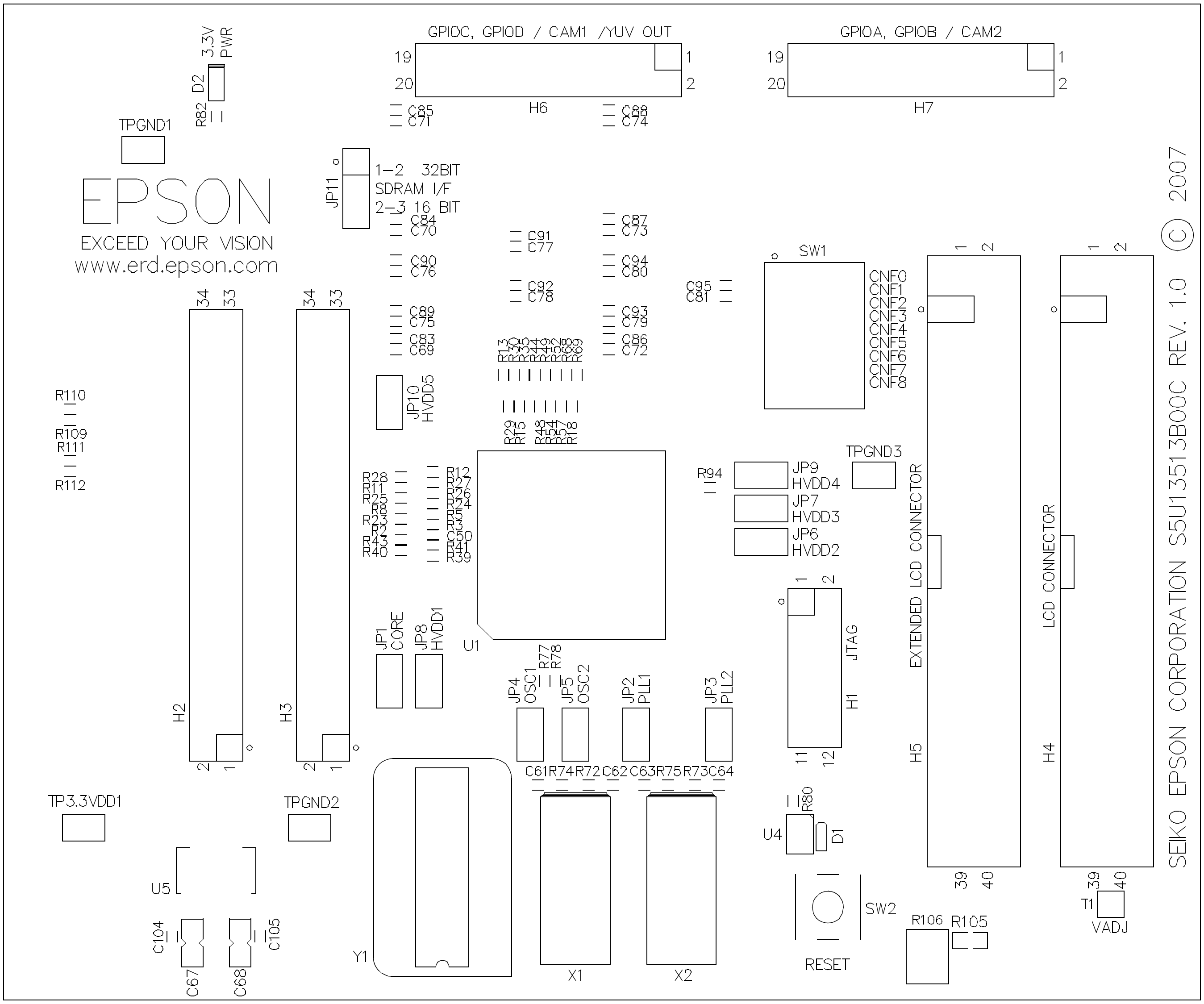


Figure 7-1: S5U13513P00C100 Board Layout - Top View

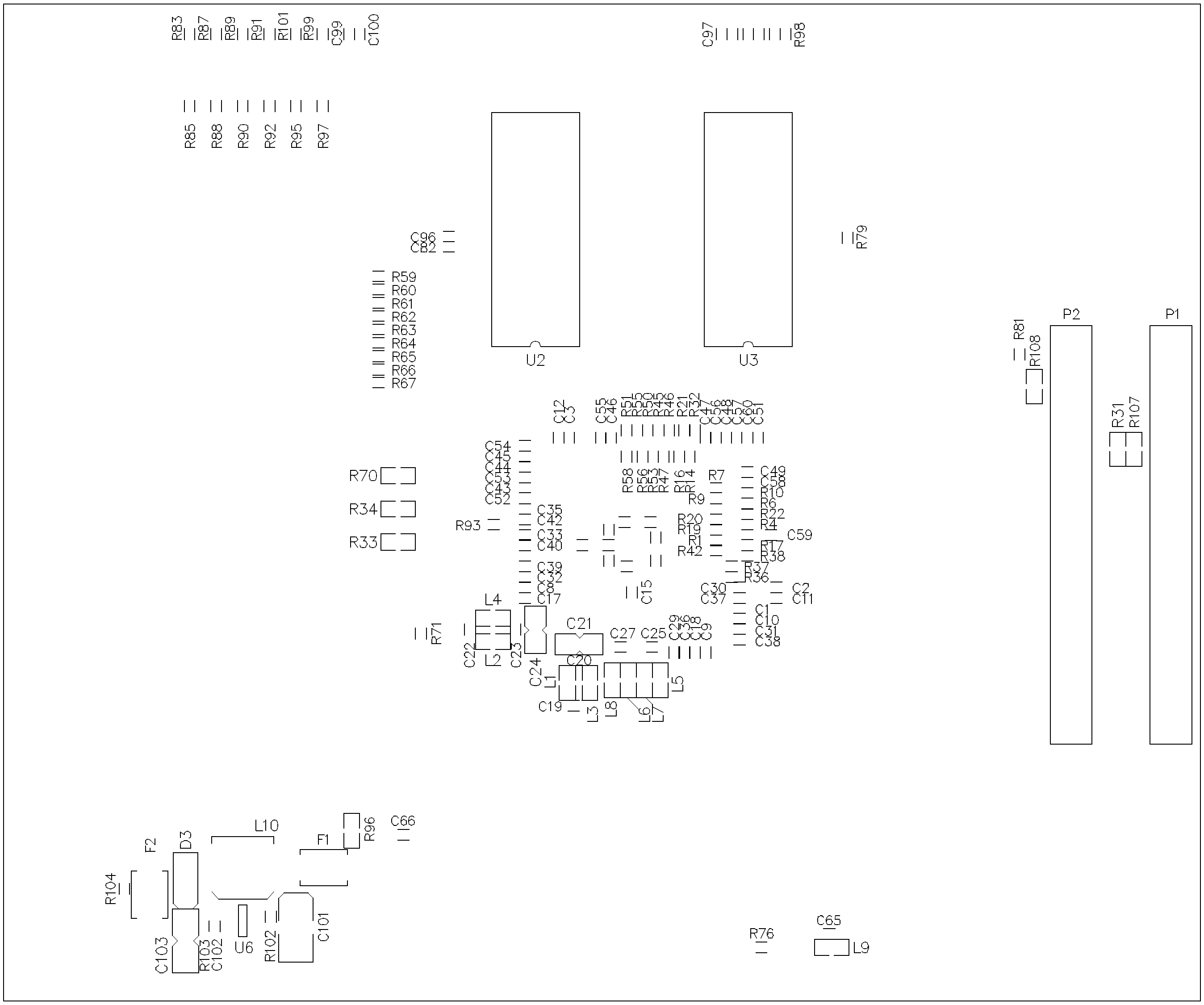


Figure 7-2: S5U13513P00C100 Board Layout - Bottom View

8 References

8.1 Documents

- Epson Research and Development, Inc., *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

8.2 Document Sources

- Epson Research and Development Website: http://www.erd.epson.com.

9 Technical Support

9.1 EPSON Display Controllers (S1D13513)

Japan
Seiko Epson Corporation
IC International Sales Group
421-8, Hino, Hino-shi
Tokyo 191-8501, Japan
Tel: 042-587-5812
Fax: 042-587-5564
http://www.epson.co.jp/

North America
Epson Electronics America, Inc.
2580 Orchard Parkway
San Jose, CA 95131, USA
Tel: (408) 922-0200
Fax: (408) 922-0238
http://www.eea.epson.com/

Taiwan
Epson Taiwan Technology & Trading Ltd.
14F, No. 7
Song Ren Road
Taipei 110, Taiwan, ROC
Tel: 02-8786-6688
Fax: 02-8786-6677
http://www.epson.com.tw/

Hong Kong
Epson Hong Kong Ltd.
20/F., Harbour Centre
25 Harbour Road
Wanchai, Hong Kong
Tel: 2585-4600
Fax: 2827-4346
http://www.epson.com.hk/

Europe
Epson Europe Electronics GmbH
Riesstrasse 15
80992 Munich, Germany
Tel: 089-14005-0
Fax: 089-14005-110
http://www.epson-electronics.de/

Singapore
Epson Singapore Pte Ltd
1 HarbourFront Place #03-02
HarbourFront Tower One
Singapore, 098633
Tel: (65) 6586-5500
Fax: (65) 6271-3182
http://www.epson.com.sg/

9.2 Ordering Information

To order the S5U13513P00C100 Evaluation Board, contact the Epson sales representative in your area and order part number **S5U13513P00C100**.

Change Record

X78A-G-003-01 Revision 1.0 - Issued: March 30, 2007

- minor edits
- updated schematics
- updated parts list
- added board layout

X78A-G-003-00 Revision 0.02

- revised manual due to design changes
- added new schematics
- added new parts list

X78A-G-003-00 Revision 0.01

- Initial draft of manual